

S/N 09/407,204

PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Shen	Examiner:	N. Parekh
Serial No.:	09/407,204	Group Art Unit:	2811
Filed:	September 28, 1999	Docket No.:	8688.128US01
Title:	SEMICONDUCTOR CHIP MODULE		

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Letter
FJONES
8-16-01VIA FACSIMILEREQUEST FOR RESETTING OF THE TIME PERIOD FOR RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action of July 5, 2001, Applicant hereby requests that the time period for responding to the Action be reset and a new Office Action issued, as the rejection under 35 USC 103(a) is unclear.

In section 2 of the Office Action, claims 1-6 have been rejected under 35 USC 103(a) as being unpatentable over Yew et al. (US Patent 6,137,164) in view of Panchou et al. (US Patent 6,040,630) and further in view of Bertin et al. (US Patent 5,977,640). However, the rejection refers to Clayton in the body of the rejection. Bertin is not mentioned. It is unclear as to whether or not the claims are being rejected in further view of Clayton (US Patent 5,731,633), Bertin, or both. Enclosed for the Examiner's convenience is a copy of the pertinent pages of the Office Action with the discrepancies highlighted.

Applicant respectfully requests that a new Office Action be issued and that the time period for responding to the Action be reset.

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If any further questions or concerns arise, the Examiner is urged to contact the undersigned at the number listed below.

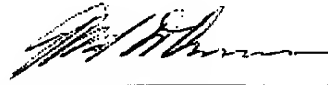
Respectfully Submitted,

MERCHANT & GOULD P.C.
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Dated

August 15, 2001

By



Michael D. Schumann
Reg. No. 30,422
MDS/CDS



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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al (US Pat. 6137164) in view of Panchou et al (US Pat. 6040630) and further in view of Bertin et al (US Pat. 5977640).

Regarding claims 1 and 2, Yew et al disclose a semiconductor stacked device/multichip module(MCM) comprising:

- a chip mounting member/printed circuit board-PCB (420 in Fig.4A) having opposite first and second surfaces (Col. 4, line 50), a set of circuit traces and a plurality of conventional vias/plated through holes (430 in Fig. 4A) that extend through the first and second surfaces and are connected to the circuit traces
- a first and second semiconductor chips (401/402 in Fig. 4A) on top and bottom surfaces of the PCB respectively and the semiconductor chips having a pad mounting surface with a plurality of contact pads/terminals (411 in Fig. 4A) provided thereon

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- a first and second conductor units including a plurality of conventional conductive contact bumps/terminals (412 in Fig. 4A; Col. 4, line 55) for electrically connecting the contact pads of the first semiconductor chip and first circuit traces, and

- plurality of solder balls/external connections (440 in Fig. 4A) disposed on one of the surfaces of the chip mounting member

(Fig. 4A; Col. 4, line 50- Col. 7, line 2).

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Yew et al disclose the first semiconductor chip being conventionally bonded to the chip mounting member/PCB using flip-chip bonding of the conductive balls/bumps (Col. 7, line 6) but fails to specify using a first dielectric tape for bonding/securing adhesively with the a plurality of holes at positions registered with the first conductor unit including a plurality contact pads/balls of the first semiconductor chip to bond and establish the electrical connection between the chip to the first circuit traces on the chip mounting member/substrate and aligning/connecting solder balls to the respective plated through holes. Panchou et al teach using a conventional attachment film/dielectric tape with a plurality of holes at positions in registration with the corresponding contact pads/balls of the chip in adhesive bonding of a flip chip device (Fig. 4 and 4a; Col. 5; Fig. 1-4). The cited reference by Clayton teaches using the conventional adhesive film/dielectric tape for bonding the first and second semiconductor chips on the circuit substrate (Fig. 18A-D; Col. 11, line 36; Col. 18, line 50) in a multichip module with wire bonding (Fig. 18C) or flip chip bonding (Fig. 18D). Clayton further teaches disposing the first circuit traces and the first semiconductor chip on the same surface of the chip mounting member/substrate and

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TO: Commissioner for Patents
Attn: Examiner Nitin Parekh
Patent Examining Corps
Facsimile Center
Washington, D.C. 20231

FROM: Michael D. Schumann

OUR REF: 8688.128US01
TELEPHONE: (612) 336.4638

Total pages, including cover letter: 5PTO FAX NUMBER 1-703-308-7722

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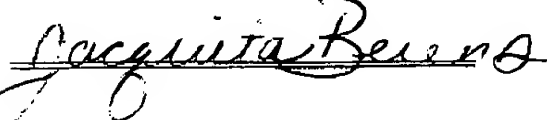
Title of Document Transmitted: Request for Resetting of the Time Period for
Response (2 pages); Copy of Pages 2 and 3 of Office Action mailed July 5, 2001

Applicant: SHEN
Serial No.: 09/407,204
Filed: September 28, 1999
Group Art Unit: 2811
Our Ref. No.: 8688.128US01

Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers, if appropriate.

By: Name: Michael D. SchumannReg. No.: 30,422

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.



Jacquita Berens
Signature

GEN033.DOT

08-15-01
Date